

a comparison circuit connected to the bus line; and

the second semiconductor device includes:

an input circuit connected to the bus line for acquiring a first bus line signal, and

a second output circuit connected to the input circuit for inverting the first bus line

signal to generate a second logical output signal, and supplying a corresponding bus

line with the second logical output signal, wherein the comparison circuit receives a

second bus line signal and compares the first logical output signal and the second bus

line signal to generate a judgment signal regarding a connection between the first

semiconductor device and the second semiconductor device.

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12. (Once Amended) The electronic device of claim 11, wherein the

semiconductor device includes a plurality of first output circuits and one of the bus lines

is a selected bus line, and the first output circuit corresponding to the selected bus line

supplies the selected bus line with the first logical output signal having a first logical

value, and the other first output circuits corresponding to the other bus lines supplies the

other bus lines with signals having a second logical value.

13. (Once Amended) The electronic device of claim 11, wherein the first

semiconductor device includes a plurality of first output circuits and at least one bus line

is adjacent to another bus line, and a first output circuit corresponding to the at least

one bus line supplies the first bus line with the first logical output signal having a first

logical value, and a first output circuit corresponding to the another bus line supplies the

another bus line with a signal having a second logical value.

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14. (Once Amended) The electronic device of claim 11, wherein the first semiconductor device includes a first group of first output circuits corresponding to a first group of the bus lines adjacent to the second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group supplies the second group of the bus lines with signals each having a second logical value.

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18. (Once Amended) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

 a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal,

 an inversion output circuit connected to the bus lines for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal, and

 a comparison circuit connected to the bus line; and

 the second semiconductor device includes:

 an input circuit connected to the bus line for acquiring a first bus line signal, and

 a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the

second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

19. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to non-selected bus lines supply the non-selected bus lines with signals each having a second logical value.

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20. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and the first output circuit corresponding to the at least one bus line supplies the at least one bus line with the first logical output signal having a first logical value, and the first output signal corresponding to the another bus line supplies the another bus line with a signal having a second logical value.

21. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a first group of the first output circuits corresponding to a first group of the bus lines adjacent to a second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group supplies the second group of the bus lines with signals each having a second logical value.

26. (Once Amended) The electronic device of claim 11, wherein:

the input circuit comprises a latch circuit that receives a logical signal supplied

a³ from the measuring semiconductor device via one of the bus lines, and

the second output circuit comprises a logical circuit connected to the latch circuit that inverts the latched logical signal to generate an inverted logical signal.

27. (Once Amended) The electronic device of claim 26, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

28. (Once Amended) An electronic device of claim 18, wherein:

the input circuit comprises a latch circuit, and

the second output circuit comprises a logical circuit connected to the latch circuit.

29. (Once Amended) The electronic device of claim 28, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

30. (Once Amended) A semiconductor device comprising:

input terminals,

output terminals,

an internal circuit,

first bus lines that connect the input terminals and the internal circuit, respectively,

second bus lines that connect the output terminals and the internal circuit, respectively, and